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10/043,974	10/19/2001	Donald Kane	2070.006800/P6928	8124

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EXAMINER

MANOSKEY, JOSEPH D

ART UNIT	PAPER NUMBER
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2113

DATE MAILED: 07/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/043,974

Applicant(s)

KANE ET AL.

Examiner

Joseph D. Manoskey

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 13 April 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-4, 10-13, 15, 19-21 and 24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4, 10-13, 15, 19-21 and 24 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 March 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Claim Objections***

1. Claims 15 and 19 are objected to because of the following informalities:

Claim 15 is dependent from now canceled claim 14, for the purposes of further examination claim 15 will be interpreted as dependent from claim 10.

Claim 19 is dependent from now canceled claim 18, for the purposes of further examination claim 19 will be interpreted as dependent from claim 10.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-4, 10-13, 15, 19-21, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al., U.S. Patent 6,480,975, hereinafter referred to as "Arimilli '975" in view of Arimilli et al. U.S. Patent 5,867,511, hereinafter referred to as "Arimilli '511".

4. Referring to claim 1, Arimilli '975 teaches a method of detecting errors in data stored in a storage device in a system (See Col. 1, lines 5-12), determining if the error is correctable (See Col. 4, lines 24-26), and making at least a portion of the directory cache unavailable to one or more resources in the system in response to determining that the error is uncorrectable (See Col. 6, lines 2-5).

Arimilli '975 discloses making at least the portion of the directory cache unavailable comprises making at least the portion of the directory cache unavailable while the system is in operation (See Arimilli '975, Col. 6, lines 2-5).

Arimilli '975 teaches determining if the error is correctable (See Col. 4, lines 24-26), this is interpreted as testing the at least a portion of the directory cache while the at least a portion of the directory cache is offline based on determining that the error is uncorrectable.

Arimilli '975 discloses a retry circuit and allowing ECC to attempt the correct the problem, this is interpreted as servicing the storage device in response to testing and then dynamically allowing access to the storage unit in response to testing the storage device (See Arimilli '975, Col. 6, lines 2-5).

Arimilli '975 does not teach wherein making at least a portion of the directory cache unavailable comprises generating a cache miss in response to a request to access the directory cache, however Arimilli '975 does teach dealing with errors in the cache, that ultimately can make the cache entry unusable (See Col. 6, lines 2-14).

Arimilli '511 cache directory that has a repair mask entry and once the entry has been set any future accesses to the cache line will be seen as a miss (See Col. 7, lines

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65-67). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the repair masking of Arimilli '511 with the directory cache of Arimilli '975. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because the allows the processor to continually run after the defect is found in the cache thus making the cache entry unusable (See Arimilli '511, Col. 7, lines 60-67).

5. Referring to claim 2, Arimilli '975 and Arimilli '511 teach all the limitations (See rejection of claim 1) including the use of ECC (error correction code) for detecting the errors (See Arimilli '975, Col. 4, lines 52-57).

6. Referring to claim 3, Arimilli '975 and Arimilli '511 disclose all the limitations (See rejection of claim 2) determining if the detected error is correctable by determining that the detected error is a multi-bit error (See Arimilli '975, Col. 4, lines 24-26).

7. Referring to claim 4, Arimilli '975 and Arimilli '511 teach all the limitations (See rejection of claim 1) including the use of parity checks and including being applied to address tags (See Arimilli '975, Col. 4, lines 43 and 54-55).

8. Referring to claim 10, Arimilli '975 discloses an apparatus comprising a directory cache adapted to store at least one entry (See Fig. 1 and Col. 4, lines 54-55). Also the apparatus includes a cache controller (See Arimilli '975, Col. 1, lines 58-60). Arimilli '975

teaches determining if an error in the directory cache is uncorrectable (See Col. 4, lines 24-26), and placing the directory cache offline in response to determining that the error is uncorrectable (See Col. 6, lines 2-5).

Arimilli '975 teaches determining if the error is correctable (See Col. 4, lines 24-26), this is interpreted as testing the at least a portion of the directory cache while the at least a portion of the directory cache is offline based on determining that the error is uncorrectable.

Arimilli '975 discloses the cache is associated with a domain, and wherein the control unit places the directory cache offline while the domain is active (See Arimilli '975, Col. 6, lines 2-5).

Arimilli '975 discloses a retry circuit and allowing ECC to attempt the correct the problem, this is interpreted as servicing the directory cache in response to testing and then dynamically placing the directory cache online in response to testing the storage device (See Arimilli '975 Col. 6, lines 2-5).

Arimilli '975 does not teach wherein placing at least a portion of the directory cache unavailable comprises generating a cache miss in response to a request to access the directory cache, however Arimilli '975 does teach dealing with errors in the cache, that ultimately can make the cache entry unusable (See Col. 6, lines 2-14).

Arimilli '511 cache directory that has a repair mask entry and once the entry has been set any future accesses to the cache line will be seen as a miss (See Col. 7, lines 65-67). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the repair masking of Arimilli '511 with the directory cache of

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Arimilli '975. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because the allows the processor to continually run after the defect is found in the cache thus making the cache entry unusable (See Arimilli '511, Col. 7, lines 60-67).

9. Referring to claim 11, Arimilli '975 and Arimilli '511 teach all the limitations (See rejection of claim 10) including the cache being set-associative (See Arimilli '975, Col. 2, lines 65-67), this interpreted as including three-way set associative.

10. Referring to claim 12, Arimilli '975 and Arimilli '511 disclose all the limitations (See rejection of claim 10) including determining if the detected error is correctable by determining that the detected error is a multi-bit error (See Arimilli '511, Col. 4, lines 24-26).

11. Referring to claim 13, Arimilli '975 and Arimilli '511 teach all the limitations (See rejection of claim 12) including the use of parity checks and including being applied to address tags (See Arimilli '975, Col. 4, lines 43 and 54-55).

12. Referring to claim 15, Arimilli '975 and Arimilli '511 teach all the limitations (See rejection of claim 14) including the cache directory having a repair mask entry and once the entry has been set any future accesses to the cache line will be seen as a miss (See Arimilli '511, Col. 7, lines 65-67).

13. Referring to claim 19, Arimilli '975 and Arimilli '511 disclose all the limitations (See rejection of claim of 15) including a retry circuit and allowing ECC to attempt the correct the problem, this is interpreted as servicing the directory cache in response to testing and then dynamically placing the directory cache online in response to testing the storage device (See Arimilli '975 Col. 6, lines 2-5).

14. Referring to claim 20, Arimilli '975 teaches a cache controller that executes instructions from a carrier medium (See Col. 1, lines 58-60). Arimilli '975 discloses determining if the detected error is correctable by determining that the detected error is a multi-bit error (See Col. 4, lines 24-26). Arimilli '975 teaches determining if an error in the directory cache is uncorrectable (See Col. 4, lines 24-26), and isolating the directory cache in response the multiple bit error (See Col. 6, lines 2-5).

Arimilli '975 teaches determining if the error is correctable (See Col. 4, lines 24-26), this is interpreted as testing the at least a portion of the directory cache while the at least a portion of the directory cache is offline based on determining that the error is uncorrectable. Arimilli '975 teaches testing the storage device in response to isolating the storage device (See Arimilli '975, Col. 4, lines 25-26).

Arimilli '975 discloses a retry circuit and allowing ECC to attempt the correct the problem, this is interpreted as servicing the directory cache in response to testing dynamically restoring the storage unit in response to testing the storage device (See Arimilli '975, Col. 6, lines 2-5).



Arimilli '975 does not teach wherein isolating at least a portion of the directory cache comprises generating a cache miss in response to a request to access the directory cache, however Arimilli '975 does teach dealing with errors in the cache, that ultimately can make the cache entry unusable (See Col. 6, lines 2-14).

Arimilli '511 cache directory that has a repair mask entry and once the entry has been set any future accesses to the cache line will be seen as a miss (See Col. 7, lines 65-67). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the repair masking of Arimilli '511 with the directory cache of Arimilli '975. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because the allows the processor to continually run after the defect is found in the cache thus making the cache entry unusable (See Arimilli '511, Col. 7, lines 60-67).

15. Referring to claim 21, Arimilli '975 and Arimilli '511 teach all the limitations (See rejection of claim 20) including the use of ECC (error correction code) for detecting the errors (See Arimilli '975, Col. 4, lines 52-57).

16. Referring to claim 24, Arimilli '975 and Arimilli '511 teach all the limitations (See rejection of claim 20) including indicating an error has occurred in reading the address tag, this is interpreted as providing a cause of the multiple-bit error (See Arimilli '975, Col. 5, lines 48-51).

***Response to Arguments***

17. Applicant's arguments, see page 6 of amendment, filed 13 April 2005, with respect to claims 20-24 have been fully considered and are persuasive. The 35 U.S.C. 101 rejection of claims 20-24 has been withdrawn.

18. Applicant's arguments, see pages 6-9 of amendment, filed 13 April 2005, with respect to the 35 U.S.C. 103(a) rejection of claim 1-8, and 10-24 have been fully considered but they are not persuasive. The examiner respectfully disagrees with the applicant that the prior art does not teach the limitations of the claims, see above rejection, and that prior art teaches permanently causing a cache miss to an access to a bad cache line. Arimilli '975 discloses a retry circuit and allowing ECC to attempt the correct the problem, this is interpreted as servicing the directory cache in response to testing dynamically restoring the storage unit in response to testing the storage device (See Arimilli '975, Col. 6, lines 2-5).

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not

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mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Manoskey whose telephone number is (571) 272-3648. The examiner can normally be reached on Mon.-Fri. (7:30am to 4pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JDM  
June 28, 2005

  
**SCOTT BADERMAN**  
**PRIMARY EXAMINER**